CCMG

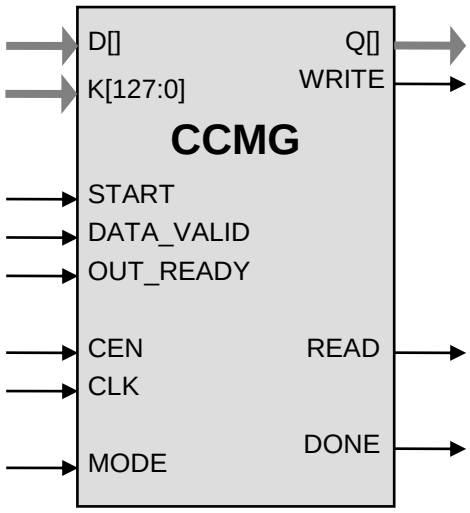
G.hn AES-CCM Core

General Description

Implementation of the new ITU G.9961 standard for home networking requires the NIST standard AES cipher in CTR and CBC modes (a.k.a. CCM) for encryption and message authentication. The CCMG AES core is tuned for G.hn applications at 3-4 Gbps data rates. The core contains the base AES core AES1 and is available for immediate licensing.

The design is fully synchronous and available in both source and netlist form.

Symbol



Key Features

Small size:
From 27,700 ASIC gates at G.hn data speeds

Completely self-contained: does not require external memory

Includes encryption, decryption, key expansion and data interface

Support for Counter Mode Encryption (CTR) operation and CCM extensions (Counter Mode with CBC MAC)

Automatic generation of key context from key data in the datastream

Flow-through design

Test bench provided

Applications

- G.hn ITU G.9661

Pin Description

Name	Type	Description
CLK	Input	Core clock signal
CEN	Input	Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.
MODE	Input	Mode. When HIGH, transmit, when LOW receive
START	Input	HIGH starting input data processing
READ	Output	Read request for the input data byte
DATA_VALID	Input	HIGH when valid data byte present on the input
WRITE	Output	Write to the output interface
OUT_READY	Input	HIGH when output interface is ready to accept data byte
D[ ]	Input	Input Data (configurable width)
Q[ ]	Output	Output Data
K[127:0]	Intput	AES encryption key
DONE	Output	Data processing completed

Function Description

The Advanced Encryption Standard (AES) algorithm is a new NIST data encryption standard as defined in the http://csrc.nist.gov/publications/fips/fips197/fips-197.pdf .

The CCMG implementation fully supports the AES algorithm for 128 bit keys in Counter Mode (CTR) method of encryption with CBC message integrity check as required by the CCMP protocol of the G.hn standard,

The core is designed for flow-through operation, with configurable-width input and output interfaces (the peak core throughput is 12.8 bits per clock). CCMG operates on the LLC frames of the G.hn standard. CCM nonce information precedes the frame in the flow of data, the key is input via dedicated pins. CCMG supports both encrypt and decrypt modes.

Implementation Results

Device Utilization and Performance

Representative area/resources figures are shown below.

Technology	Area / Resources
TSMC 65 nm	27,700 gates

.

Export Permits

US Bureau of Industry and Security has assigned the export control classification number 5E002 to the AES1 core. The core is eligible for the license exception ENC under section 740.17(A) and (B)(1) of the export administration regulations. See the IP Cores, Inc. licensing basics page, http://ipcores.com/exportinformation.htm, for links to US government sites and more details.

Deliverables

HDL Source Licenses

- Synthesizable Verilog RTL source code
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Simulation script
- Synthesis script
- User Documentation

Contact Information

IP Cores, Inc.
3731 Middlefield Rd.
Palo Alto, CA 94303, USA
Phone: +1 (650) 815-7996
E-mail: info@ipcores.com
www.ipcores.com