

### General Description

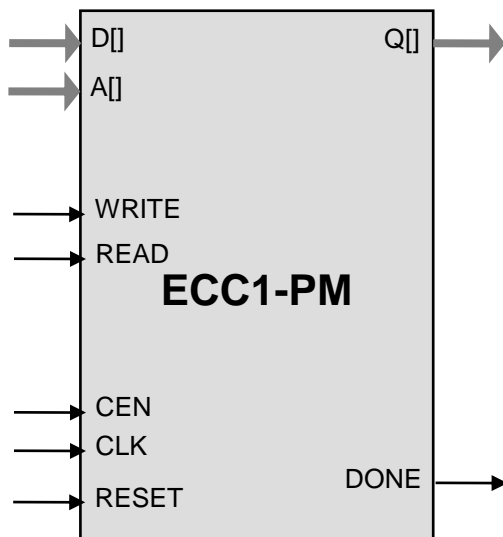
Elliptic Curve Cryptography (ECC) is a public-key cryptographic technology that uses the mathematics of so called “elliptic curves” and it is a part of the “Suite B” of cryptographic algorithms approved by the NSA.

Since ECC requires fewer bits than RSA to achieve the same cipher strength, it is frequently used in embedded applications. The operations necessary for the ECC cannot be efficiently implemented on an embedded CPU, however, typically requiring hundreds of milliseconds of the CPU time for signature verification.

ECC1-PM implements by far the most time-consuming operation of the ECC cryptography: so called “point multiplication” to enable low-power operation of the battery-powered devices.

The design is fully synchronous and available in multiple configurations varying in bus widths, set of elliptic curves supported and throughput.

### Symbol



### Key Features

Small size: ECC1-PW starts from less than 10K ASIC gates (intermediate result storage memory required; size depends on the core configuration)

Implements the computationally demanding parts of ECC public key cryptography for long life battery powered applications

Support for ECC binary fields  $2^{163}$ ,  $2^{233}$ ,  $2^{283}$ ,  $2^{409}$ , and  $2^{571}$

Microprocessor-friendly interface

Test bench provided

### Applications

- Secure communications systems
- RFID
- Implantable medical devices
- Digital Rights Management (DRM) for battery powered electronics
- Elliptic Curve Diffie-Hellman (EC-DH) standard ANSI X9.63
- Elliptic Curve Digital Signature Algorithm (EC-DSA) standard ANSI X9.62
- B and K elliptic curves (163, 233, 283, 409, 571) defined by NIST
- IEEE P1363 curves over binary fields  $GF(2^m)$
- TLS implementations per RFC 4492
- Cryptographic messaging per RFC 3278

### Pin Description

Name	Type	Description
CLK	Input	Core clock signal
CEN	Input	Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.
RESET	Input	HIGH level asynchronously resets the core
READ	Input	Read signal for the interface
WRITE	Input	Write signal for the interface
DONE	Output	HIGH level indicates a completion of computation
D[]	Input	Input Data
A[]	Input	Address
Q[]	Output	Output Data

### Function Description

The core implements the Point Multiplication operation of the ECC cryptography  $Q = kP$ . The operands for the multiplication:  $k$ ,  $P_x$ ,  $P_y$  are programmed through the microprocessor interface. The curve parameters  $a/b$  are selected through the microprocessor interface and the calculation is started. Once the operation is complete, the result  $Q_x$ ,  $Q_y$  can be read through the interface.

### Export Permits

The core is subject to the US export regulations. See the IP Cores, Inc. licensing basics page, [http://ipcores.com/export\\_licensing.htm](http://ipcores.com/export_licensing.htm), for links to US government sites and licensing details.

### Deliverables

#### HDL Source Licenses

- Synthesizable Verilog RTL source code
- Software modules for a complete ECC implementation (optional)
- Verilog testbench (self-checking)
- Software modules test harness
- Vectors for testbench and harness
- Expected results
- User Documentation

#### Netlist Licenses

- Post-synthesis EDIF
- Testbench (self-checking)
- Vectors for testbench
- Expected results

### Contact Information

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